

10/089425

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PATENT NUMBER and
ISSUE DATE

U.S. UTILITY Patent Application

APPL N°JM 10089425	FILING DATE 07/29/2002	CLASS 563 307	SUBCLASS 147	GAU 2836 2826	EXAMINER Vn
**APPLICANTS: Eder Stefan;					
**CONTINUING DATA VERIFIED: THIS APPLICATION IS A 371 OF PCT/DE00/01737 05/29/2000 <i>ok. BL</i>					
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** FOREIGN APPLICATIONS VERIFIED: GERMANY 199 25 422.2 06/02/1999 <i>ok. BL</i>					
PG-PUB <input type="checkbox"/> DO NOT PUBLISH <input type="checkbox"/>		RESCIND <input type="checkbox"/>			
Foreign priority claimed <input checked="" type="checkbox"/> yes <input type="checkbox"/> no		35 USC 119 conditions met <input checked="" type="checkbox"/> yes <input type="checkbox"/> no		ATTORNEY DOCKET NO	
Verified and Acknowledged Examiners's initials <i>BL</i>				Mic.6688	
TITLE : Circuit comprising an integrated switching circuit and a voltage regulating circuit					
<small>U.S. DEPT. OF COMM./PAT. & TM.-PTO-436L (Rev. 12-94)</small>					

NOTICE OF ALLOWANCE MAILED		Assistant Examiner	CLAIMS ALLOWED		
			Total Claims	Print Claim for O.G.	
ISSUE FEE		Primary Examiner	DRAWING		
Amount Due	Date Paid		Sheets Drwg.	Figs. Drwg.	Print Fig.
<input type="checkbox"/> TERMINAL DISCLAIMER		PREPARED FOR ISSUE	Application Examiner		
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